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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,156	01/20/2004	Naohito Kojima	2102487-991320	4963

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/762,156	KOJIMA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *7 and 9-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Igarashi et al. (6,262,487) in view of Applicant Admitted Prior Art (AAPA).

Igarashi et al. teach in figure 13C and related text a semiconductor integrated circuit comprising:

a function block 80 (the bottom cell block) arranged on a substrate;

a first buffereing cell 183 arranged outside of the function block (located outside the bottom cell block and inside the second cell block) and adjacent to a first side of the function block;

a second buffering cell (since there are plurality of cells 183) arranged outside of the function block (located outside the bottom cell block and inside the third cell block) and adjacent to a second side adjacent to the first side of the function block and

a signal wiring 173 passing over the function block obliquely relative to the first side and the second side.

Igarashi et al. do not explicitly state that the signal wiring connecting the first buffering cell and the second buffering cell.

Igarashi et al. teach in figure 6A and related text a signal wiring 23 is connected to a buffering cell 20.

AAPA teaches in figure 1 and related text a wiring 4b connecting the first buffering cell 3b1 and the second buffering cell 3b2.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect the signal wiring to the first buffering cell and the second buffering cell in Igarashi et al.'s device in order to improve the device characteristics by providing electrical connections between the buffereing cells.

Regarding claims 2-6, Igarashi et al. teach in figures 4 and 10 and related text a first signal wiring 1 extending in a generally horizontal direction, which is arranged inside the function block and extends obliquely relative to the signal wiring; and a second signal wiring 2 extending in a generally verical direction generally perpendicular to the horizontal direcdon, which is arranged inside the function block and generally perpendicular to the first signal wiring and extends obliquely relative to the signal wiring, wherein

the signal wiring is arranged in a layer higher than the layer in which the first signal wiring and the second signal wiring are arranged, wherein

the signal wiring has an intersecting angle either 45 degrees and 135 degrees relative to either of the first signal wiring and the second signal wiring, wherein

the signal wiring is a global signal wiring including one of a data bus and an address bus, wherein

the first buffering cell and the second buffering cell are arranged outside of the function block.

Regarding claim 8, Igarashi et al. and AAPA teach substantially the entire claimed structure, as applied to claim 1 above. Igarashi et al. do not teach that each of a plurality of signal wirings have a length shorter than a length of a side of the function block.

AAPA teaches in figure 1 and related text a signal wiring 4b having a length shorter than a length of a side of the function block 2.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the plurality of signal wirings having a length shorter than a length of a side of the function block in Igarashi et al.'s device in order to reduce the wiring delay and to reduce the cross-talk noise. Note that the length of the signal wiring is an important criteria in the design of the device.

Response to Arguments

Applicant argues that Igarashi et al. teach in figure 13C and related text a first buffereing cell 183 arranged inside of the function block 80 and not outside the function block, as required by claims 1 and 8.

Igarashi et al. teach in figure 13C and related text a function block 80 (the bottom cell block) and a first buffereing cell 183 arranged outside said function block, because

the first buffereing cell 183 is located outside the boundaries of bottom function block 80. Note that the broad recitation of the claims does not require all the buffereing cells to be arranged outside the function blocks.

Applicant argues that Igarashi et al. do not teach a signal wiring connecting the first buffering cell and the second buffering cell.

The examiner agrees that Igarashi et al. do not explicitly state that the signal wiring connecting the first buffering cell and the second buffering cell. However, Igarashi et al. teach in figure 6A and related text a signal wiring 23 is connected to a buffering cell 20. Figure 13C of Igarashi et al. depicts a signal wiring 173 passing over all the function blocks and the buffering cells obliquely relative to the first side and the second side. Therefore, since a signal wiring is connected to a buffering cell (figure 6A), and signal wiring 173 is passing over ad connecting all the function blocks and the buffering cells, then the signal wiring must electrically connect the first buffering cell and the second buffering cell in order to operate the device.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
2/5/07

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PRIMARY EXAMINER
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